UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/080,406	02/25/2002	Mikihito Sugiura	21900/0047	8338

30678 7590 03/22/2006

CONNOLLY BOVE LODGE & HUTZ LLP
SUITE 800
1990 M STREET NW
WASHINGTON, DC 20036-3425

EXAMINER	
MERED, HABTE	
ART UNIT	**PAPER NUMBER**
2616	

DATE MAILED: 03/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/080,406	SUGIURA ET AL.	
	Examiner	Art Unit	
	Habte Mered	2662	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 February 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 February 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *02/19/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-35 are pending.

Specification

2. The disclosure is objected to because of the following informalities:

Page 2, Line 14 indicates the label RAM 252 while the corresponding label in Figure 19 is shown as RAM 251.

Appropriate correction is required.

Drawings

3. The drawings are objected to because in Figure 6 the label "Mew Header Data" should be replaced by "New Header Data". Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of

any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. **Claims 1, 2, 9-11, 19-24, 33, 34 and 35** are rejected under 35 U.S.C. 103(a) as being unpatentable over Nogami et al (US 6, 781, 994), hereinafter referred to as Nogami, in view of Kloth et al (US 6, 570, 877), hereinafter referred to as Kloth, and Park (Yeoung-Ho Park, "Bi-directional 3-port ATM CAM supporting fast look-up and reduced cycle time", IEEE, 1996).

Nogami discloses a method of distributing ATM cells to output ports based upon destination information using ATM switch core and IP Forwarding.

6. Regarding **claims 1, 33, and 35**, Nogami discloses an ATM header conversion circuit and method **(See Figure 14 and Column 8, Lines 17-67 and Column 9: Lines 1-32; Figure 37 and Column 35, Lines 14-19; and Figure 44 and Column 39, Lines 49-67)** comprising: entry data storage means for storing, as entry data, first and second ATM header data paired at each of a plurality of addresses; **(Element 415 in Figures 37, 39, and 40 (A and B) is a table in memory and serves as a data storage. Clearly two ATM headers reside in the table and are namely VPI/VCI's of the input and output side. See also Column 35, Lines 14-24.)**

partial collation means for partially collating inputted header data with one of the first and second ATM header data stored in the entry data storage means for each address on the basis of a designation signal representative of a collation position of the ATM header data being converted, and for outputting a collation result for each address **(See Column 35:Lines 25-32; Figure 38, step A12; and Figure 39. Since a masking operation is conducted in Nogami's system, whenever there is a match, it is inherent for the system to output a coalition result for each address. Nogami's system is capable of performing partial as well as full masking of the header data to be compared.)**; and header outputting means **(See element 555 of Figure 14)** for outputting, as converted ATM header data, the other of the first and second ATM header data at the address extracted by the address extraction means **(Element 553 in Figure 14)**, from the entry data storage means **(i.e. input-port conversion table of Figure 14) (See also Column 35, Lines 33-40, 50-57, and 60-66; Figure 38, step A14; Figure 41, step B15)**.

7. Regarding **claims 10 and 34**, Nogami discloses an ATM header conversion circuit and method **(See Figure 14 and Column 8, Lines 17-67 and Column 9: Lines 1-32; Figure 37 and Column 35, Lines 14-19; and Figure 44 and Column 39, Lines 49-67)** comprising: entry data storage means for storing ATM header data, which remain unchanged before and after conversion, as entry data in a state associated with first and second addresses paired; **(Element 415 in Figures 37, 39, and 40 (A ,B) is a table in memory and serves as a data storage. Clearly two ATM headers reside in**

the table and are namely VPI/VCI's of the input and output side. See also Column 35, Lines 14-24.)

full collation means for fully collating inputted header data with the ATM header data, stored in the entry data storage means, at each of the pairs of first and second addresses to output a collation result at each of the pairs of first and second addresses; **(Nogami's system is capable of performing partial as well as full masking of the header data to be compared. See Column 35:Lines 25-32; Figure 38, step A12; and Figure 39. Since a masking operation is conducted in Nogami's system, whenever there is a match, it is inherent for the system to output a coalition result for each address.)**;

converted ATM header storage means for previously storing the ATM header data after conversion in a state associated with the first and second addresses in the entry data storage means **(See Column 35: 52-59)**;

and readout means for selecting one of the first and second addresses extracted in the address extraction means to read out the ATM header data at the selected address from the converted ATM header storage means. **(See also Column 35, Lines 33-40, 50-57, and 60-66; Figure 38, step A14; Figure 41, step B15)**.

8. With respect to **claims 1, 10, 33, 34 and 35**, Nogami, however, fails to expressly disclose address extraction means for retrieving an address of a matched result in the header conversion table.

Kloth discloses a search engine for forwarding table content addressable memory.

Kloth teaches address extraction means for retrieving an address of a matched result in the header conversion table. (**Kloth discloses in Column 4, Lines 36-49 the Forwarding table CAM (i.e. entry data storage means) shown as element 12 in Figure 1 is accessed by using a "key" that is a masked subset of entries in the Forwarding table CAM. The search engine 18 of Figure 1 is the address extraction means as illustrated in Column 10, Lines 6-12 and whenever there is a match the state bits in the VRAM (element 26 in Figure 1) are modified for that entry (i.e. making it an effective indication of a collation result) and eventually the address of that entry is obtained by the search engine and placed in the search FIFO which is element 24 in Figure 1. Please see also Column 7, Lines 4-14; Column 8, Lines 14-24 and 42-67)**

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Nogami's header conversion means to incorporate an address extraction means. A processor accessing the header conversion table has limited number of instruction cycles that it may use for searching a large table in a given amount of time. The motivation to use an address extractor is to allow the processor search a large header conversion table quickly without consuming extra scarce processor instruction cycles for retrieving addresses of matched entries as illustrated by Kloth in Column 2, Lines 14-25. The address extractor retrieves the addresses after the table search is completed based on the matched entries indications.

9. With respect to **claims 1, 10, 11, 33, 34 and 35**, Nogami fails to disclose his header conversion mechanism is bidirectional.

Park discloses a bidirectional 3-port ATM CAM supporting fast look-up and reduced cycle time.

Park discloses a header conversion mechanism and is fully bidirectional. **(See Figure 4; Page 162, 2nd column, lines 1-10; and abstract)**

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Nogami's header conversion means to make it bidirectional. The motivation for using a bidirectional header conversion circuit reduces circuitry by using the same hardware for both input and output sides and therefore makes the whole communication system cheaper.

10. Regarding **claim 2**, Nogami discloses an ATM header conversion circuit, wherein the designation signal representative of the collation position of one of the first and second ATM header data is generated in units of bits, and the partial collation means collates the inputted header data with one of the first and second ATM header data in units of bits. **(See Column 35, Lines 25-32)**

11. Regarding **claim 9**, Nogami teaches an ATM header conversion circuit, wherein the header outputting means is made to output, in addition to the converted ATM header data, a corresponding address in the entry data storage means. **(See Column 35, Lines 48-59. Certainly Nogami teaches outputting the converted ATM header data and this particular header data is stored in memory and it is inherent for any system like Nogami's to obtain the address in memory first to fetch the data because to access any memory for reading and writing purposes always require prior knowledge of the address.)**

12. Regarding **claim 19**, Nogami teaches an ATM header conversion circuit, wherein connection information is added to the entry data and stored in the entry data storage means. **(See Figure 39 – the header conversion table 415 has line number and VPI/VCI as connection information.)**

13. Regarding **claim 20**, Nogami teaches an ATM header conversion circuit, wherein the connection information, together with the converted header data corresponding to the inputted header data is outputted on the basis of the designation signal representative of the collation position of the ATM header data being converted. **(See Figure 39 – the header conversion table 415 has line number and VPI/VCI as connection information. It has already been established in the rejection of claims 1 and 10 that Nogami uses masking and when there is a match everything associated with the input header matched is outputted and may contain line number or VPI/VCI or other connection information as shown in Figure 39.)**

14. Regarding **claims 21 and 22**, Nogami teaches an ATM header conversion circuit, wherein, the ATM header data stored in the entry data storage means, a VPI/VCI inhibited as input in a system is set as an initial value. **(Nogami's table is pre-populated and therefore has a default value as seen in Figure 39. The Examiner is not clear on what is meant by "VPI/VCI inhibited" and assumes it to mean a value that cannot be overwritten.)**

15. Regarding **claims 23 and 24**, Nogami teaches that an ATM header conversion circuit, wherein, the ATM header data stored in the entry data storage means, a VPI/VCI which is not required to be registered is set as an initial value. **(Nogami's table is pre-**

populated and therefore has a default value as seen in Figure 39. The Examiner is not clear on what is meant by "VPI/VCI inhibited" and assumes it to mean a value that cannot be overwritten. However determining whether to set a non-registered connection, as initial value is strictly an operation issue.)

16. **Claims 3-8** are rejected under 35 U.S.C. 103(a) as being unpatentable over Nogami in view of Kloth and Park as applied to claim 1 above, and further in view of Khanna et al (US 6, 539, 455), hereinafter referred to as Khanna.

17. Regarding **claims 3-5**, the combination of Nogami, Kloth, and Park, teaches all aspects of the claimed invention as set forth in the rejection of claim 1 but does not disclose the ATM header data is masked, stored, and generated in unit of word.

Khanna discloses a method and apparatus for determining an exact match in a ternary content addressable memory device.

Khanna discloses in his system ATM header data is masked, stored, and generated in units of word. **(See Column 6, Lines 27-45 and Figure 3, element 302. Khanna shows the masking and storing in the CAM table is done in units of words.)**

18. Regarding **claims 6-8**, the combination of Nogami, Kloth, and Park, teaches all aspects of the claimed invention as set forth in the rejection of claim 1 but does not disclose the number of bits allocated to one word is variable.

Khanna discloses the number of bits allocated to one word is variable. **(See Column 6, Lines 27-45 and Figure 3, element 302. Khanna shows the masking and storing in the CAM table is done in units of words. The size of a word in**

computer science by definition is variable. The definition of word from any version of Newton telecom dictionary states as "a collection of bits the computer recognizes as a basic information unit and uses in its operation and usually defined by the number of bits contained in it, e.g. 5, 8, 16, or 32 bits".)

19. With respects to **claims 3-8**, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Nogami's header conversion means to make it mask, store and generate converted header data in units of words. The motivation being implementation of circuits that use units of words instead of units of bits require a reduced amount of hardware and are therefore cheaper to implement.

20. **Claims 12-18** are rejected under 35 U.S.C. 103(a) as being unpatentable over Nogami in view of Kloth and Park as applied to claims 1 and 10 above, and further in view of Uchida (US 5, 930, 477), hereinafter referred to as Uchida.

Uchida discloses a header conversion method and apparatus that has header conversion table stored in a common storing unit shared by several input ports.

21. Regarding **claims 12 and 13**, the combination of Nogami, Kloth, and Park, teaches all aspects of the claimed invention as set forth in the rejection of claims 1 and claims 10 respectively but does not disclose the ATM header conversion circuit, further comprising a connection whose one side has a plurality of divided ports so that addresses in the entry data storage means correspond to the numbers of the ports, respectively.

Uchida teaches that the ATM header conversion circuit, further comprising a connection whose one side has a plurality of divided ports so that addresses in the entry

data storage means correspond to the numbers of the ports, respectively. **(See Figure 6 and Column 8, Lines 11-31. Clearly in Figure 6 Uchida shows that a storage containing header conversion table is shared by many input ports and it is inherent for the addresses of the input header entries stored in the data storage to correspond to the input port numbers as further shown in Figure 12 B.)**

22. Regarding **claims 14 and 15**, the combination of Nogami, Kloth, and Park, teaches all aspects of the claimed invention as set forth in the rejection of claims 1 and claims 10 respectively but does not disclose the ATM header conversion circuit, further comprising a connection whose one side has a plurality of divided ports, and addresses in the entry data storage means include the numbers of the ports, respectively.

Uchida teaches that the ATM header conversion circuit, further comprising a connection whose one side has a plurality of divided ports, and addresses in the entry data storage means include the numbers of the ports, respectively. **(See Figures 12A-C and Figures 17A-C. See Column 13, Lines 34-50 and 64-67; Column 14, Lines 1-10; and Column 20, Lines 1-3.)**

23. Regarding **claim 16**, the combination of Nogami, Kloth, and Park, teaches all aspects of the claimed invention as set forth in the rejection of claim1 including collating on the basis of the designation signal representative of the collation position of the ATM header data being converted but does not disclose an ATM header conversion circuit, wherein header data inputted through one non-divided side of the connection, and the ATM header data converted is outputted to one of the plurality of

divided ports of the other side of connection on the basis of the port number included in the address.

Uchida discloses an ATM header conversion circuit, wherein header data inputted through one non-divided side of the connection, and the ATM header data converted is outputted to one of the plurality of divided ports of the other side of connection on the basis of the port number included in the address. **(See Figure 2, elements 103-1, 103-2, and 103-3 and further this limitation is a common practice to any switch including ATM switch. See Figures 12A-C and Figures 17A-C. See Column 13, Lines 34-50 and 64-67; Column 14, Lines 1-10; and Column 20, Lines 1-3.)**

24. Regarding **claims 17 and 18**, the combination of Nogami, Kloth, and Park, teaches all aspects of the claimed invention as set forth in the rejection of claim1 including partially collating on the basis of the designation signal representative of the collation position of the ATM header data being converted but does not disclose an ATM header conversion circuit, wherein the port numbers are added to the ATM header data on the divided side of the connection and stored in the entry data storage means.

Uchida discloses an ATM header conversion circuit, wherein the port numbers are added to the ATM header data on the divided side of the connection and stored in the entry data storage means. **(See Figure 2, elements 101-1, 101-2, and 101-3; Figures 12A-C and Figures 17A-C; See also Column 13, Lines 34-50 and 64-67; Column 14, Lines 1-10; and Column 20, Lines 1-3.)**

25. With respect to **claims 12-18**, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Nogami's header conversion means in such a way as to share the data storage containing the header conversion table amongst several input ports. The motivation is to reduce hardware circuits by using one central memory to store the header conversion table which will make the system cheap by not requiring at each input a circuit and memory to store a version of the header conversion table and a further motivation is to prevent underutilization of hardware in a distributed system (i.e. tables being located at every input like Nogami's system) as opposed to a central system (i.e. a central data storage as taught by Uchida) as further illustrated by Uchida in Column 3, Lines 45-60.

26. **Claims 25-32** are rejected under 35 U.S.C. 103(a) as being unpatentable over Nogami in view of Kloth and Park as applied to claims 1 and 10 above, and further in view of Kalapathy et al (US 6, 810, 037), hereinafter referred to as Kalapathy and Schzukin et al (US 6, 591, 317), hereinafter referred to as Schzukin.

27. Regarding **claims 25-32**, the combination of Nogami, Kloth, and Park, teaches all aspects of the claimed invention as set forth in the rejection of claims 1 and claims 10 respectively but does not disclose dividing the searching of the header conversion table to be dependent on the positions of the elements populating the table being odd or even. The combination of Nogami, Kloth, and Park, also fail to disclose that there is a counting means associated with each entry or tuple or position of the header conversion table.

Kalapathy discloses the apparatus and method for sorted table binary search acceleration.

Kalapathy discloses that dividing the searching of the header conversion table to be dependent on the positions of the elements populating the table being odd or even. **(See Column 1, Lines 35-50; Figure 39; and Column 24, Lines 10-41. Kalapathy also discloses that counters are provided to count full matches and partial matches as illustrated in Column 38, Lines 1-10. Unlike the Applicant's method a single counter is used per filter to count multiple matches.)**

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Nogami's header conversion means to incorporate a table searching method of searching even and odd entries separately. The motivation is that any system, including Nogami's, is concerned about the access and data retrieval speed of a large table like a header conversion table and Kalapathy addresses the concern by providing a method that breaks the search of a single table in two parts and indicates its advantages in Column 30, Lines 20-25.

Schzukin discloses a queue incorporating a counter per entry.

Schzukin discloses that there is a counting means associated with each entry or tuple or position of the header conversion table. **(See Figure 4, element 66 and Column 2, Lines 20-30. Schzukin also shows in Column 2, Lines 48-51 that his method is also applicable to queues with large number entries such as CAMs. Since each counter has the count of multiple matches for a specific entry in the table summing the counters at each stage does not add a unique value. However**

if the total count of multiple matches is desired it is straightforward to obtain the individual result from each counter and determine the total sum.)

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Nogami's header conversion means to incorporate a counting means associated with each entry of the header conversion table. The motivation is that any system including Nogami's that uses masking technique when searching a large table will have to address detecting multiple matches and Nogami fails to do so but Schzukin describes the means to detect multiple matches in Column 2, Lines 20-30 and 48-51.

Conclusion

28. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Habte Mered whose telephone number is 571 272 6046. The examiner can normally be reached on Monday to Friday 9:30AM to 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hassan Kizou can be reached on 571 272 3088. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Habte Mered
03-10-2006

HASSAN KIZOU
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600